# CSP Reliability for Single- and Double-Sided Assemblies

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## INTRODUCTION

This paper reviews the package trend towards further miniaturization of emerging chip scale package (CSP). The industry definition of CSP has evolved towards further miniaturization as technology and infrastructure for finer pitch become more readily available. To keep up with such definition, CSPs are considered to be miniature new packages that industry is starting to implement, and there are many unresolved technical issues associated with their implementation. One key issue yet to be fully addressed is the CSP interconnection reliability. Understanding quality and reliability issues associated with implementation of CSPs were the main objective of the JPL-led CSP Consortium with representative from government agencies and private companies. Our experience in the areas of technology implementation challenges, including design and building both standard and microvia boards, and assembly of two types of test vehicles are presented. Preliminary thermal cycling test results under four environmental conditions are also presented. Finally, thermal cycling test results for single and double- sided assemblies were compared to limited data in literature data.

## INDUSTRY AND "EXPERT" DEFINITION OF CSP

Although the expression "CSP" is widely used by industry both suppliers and users, its definition had evolved as the technology has matured. At the start of the package's introduction into the market, a very precise definition was adopted by a group of industry experts. CSP was defined as a package that is up to 1.2 or 1.5 times larger than the perimeter or the area of the die. Soon, it became apparent that suppliers were using the term CSP to promote a miniature version of a previous package.

A rapid transition to a much lower size was difficult both for package suppliers and end users. Suppliers had difficulty in building such packages whereas the users had difficulties in accommodating the need for the new microvia printed circuit board (PWB), chiefly, because of routing requirements and its increased cost. Other issues for accepting the "interim definition" by industry included needed maturity in assembly and infrastructure. For example, the use of pitches other than 0.5 mm, including 0.75 and 0.65, was aimed at using a standard PWB design rather than a microvia build to avoid the elevated cost of the latter.

The "expert definition" undermines one of the key purpose of the packages allowing for die shrinkage. If die shrinkage is acceptable for the package to retain the footprint, then a decrease in die size for the same CSP will change the term CSP for that package.

Therefore, in reality, CSPs are miniature new packages that industry is starting to implement, and there are many unresolved technical issues associated with their implementation. Technical issues themselves also change as packages mature. For example, in early 1997, packages with 1 mm pitch and lower were the dominant CSPs, whereas in early 1998 packages with 0.8 mm and lower became the norm for CSPs. New issues included the use of flip chip die rather than wire bond die in the CSP. Flip chip failure within the package is a potential new failure mechanism that needs to be considered.

### Survey by JEDED and Experience on CSP Availability

Figure 1 shows the results of surveys from JEDEC and EIAJ team members adapted from data presented in reference 1 . Surveys done in 1998 regarding the status of activity in development and production of grid CSPs. For CSPs with low I/Os (<100), both US (JEDEC) and Japan (EIAJ) have approximately similar activities. This is not true for high I/O between 100 to 300, and above 300 I/Os. For higher I/O ranges, EIAJ activities become two to three times larger than JEDEC. One JEDEC member reported development of package with 0.4 mm pitch with about in 500 I/O range.

The JPL-CSP Consortium experience on use of daisy chain for characterization of reliability followed the above package I/O and pitch trends. CSP availability in daisy chain for the attachment reliability characterization was one of the challenging issues. For example, at the start of the program, in early 1997, I/Os ranged from 12 to 540 to meet the short and longer term applications. The 540 I/O/ 0.5 mm package was dropped by the manufacturer prior to the trial test vehicle assembly. Three other higher I/O with 0.5 mm pitch were not delivered. For example, a hard metric, 0.5 mm CSP package with 188 I/Os having reliability data given by the supplier for its English pitch version was among these three packages. The supplier was unable to meet our last build scheduled in late 1998.

Lack of delivery clearly indicate that the package suppliers were struggling to build CSPs with 0.5 mm pitch, especially with high I/O counts. The majority of the CSPs of the next phase of the CSP, started in early 1998, program have pitches of 0.8 mm, in agreement with JEDE survey. In this phase, there are a few high I/O CSPs with 0.5 mm pitch. This indicates that industry is starting to be more comfortable with moving towards a tighter pitch at higher I/O as also was found by the survey.

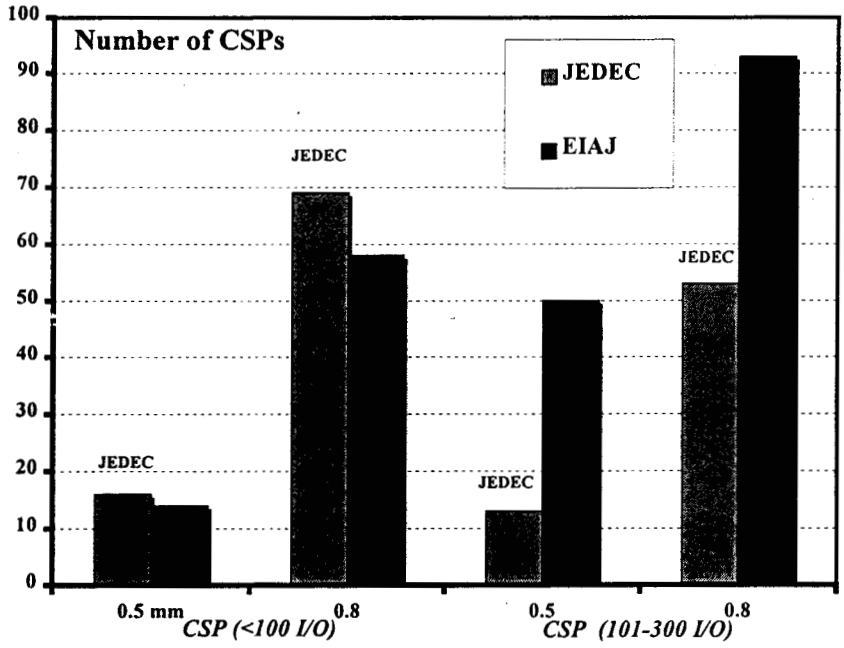


**Figure 1 Package I/O and Pitch for US and Japan**

## CSP IMPLEMENTATION CHALLENGES

The JPL-led CSP consortia of enterprises representing government agencies and private companies have jointed together to pool in-kind resources for developing the quality and reliability of chip scale packages (CSPs) for a variety of projects. In the process of building the JPL-led consortia test vehicles [2], numerous challenges were identified. The thought processes for the first test vehicle started in late 1996, when very few packages were available for evaluation. The design for the second test vehicle initiated in mid 1998, when a much larger number of CSPs were available, estimated to be nearly fifty types. Although CSPs' rapid growth has eased package availability, its implementation, especially for high reliability applications, requires establishment of many technical issues including assurance for quality and confidence in reliability, as well as development of the necessary infrastructure.

In the following, key challenges for package and PWB design, and assembly of test vehicles will be presented. Also, the most update environmental test results for CSPs and their assemblies will be given.

- Lack of Daisy Chain Package Availability: CSP availability in daisy chain for the attachment reliability characterization was one of the challenging issues at the start of the program in early 1997. At the start of the program we had planned for sixteen packages, I/Os ranged from 12 to 540 to meet the short and longer term applications.. Because of lack of delivery, the total of CSPs reduced to ten with and I/O package became a CSP with 275 I/Os.

- Lack of design guidelines and standards on various elements of CSPs were not available. For example, There was no information on pad design relative to package pad for achieving optimum reliability.

- Need for Microvia PWB: The standard PWB design could be used for low I/O CSPs. Build up (microvia) board technology is required for higher I/O CSPs in product with active die. For daisy chain packages, it is possible to design high I/O on a standard board. Board design guidelines are needed, especially for the build up (microvia) configuration.

- I/O Limitation: There were a number of packages from low I/O (<50) to higher I/Os (about 500) for characterization. It became apparent that for the near future, 1-3 years, the dominant packages would be those with less than 50 I/Os.

**CSP Test Vehicle Design**

The Consortium agreed to concentrate on the following aspects of CSP technology after numerous workshops, meetings, and weekly teleconferences.

**Package** — Ten packages from 28 to 275 as listed in Table 1. The TSOP was used as control.

**Printed Wiring Board (PWB) Materials and Build** — Both FR-4 and BT (Bismaleimide Triazine) materials were available in the resin copper coated form for evaluation. High temperature FR-4 and Thermount® were also included. The boards were double sided, standard and microvia. With our test matrix design, direct reliability comparison between the two board technologies as well as double side processing is possible. In designing daisy chains, it became apparent that the standard PWB technology could not be used for routing the majority of packages.

**Table 1 CSP Package Configurations Matrix**

| Package ID | Package. Type | Package Size (mm) | Pad Size (mm) | Pitch (mm) | I/O Count | Package. Thickness (mm) | Ball Dia (mm) |
|---|---|---|---|---|---|---|---|
| A | Low I/O Wafer | 1.6 x 3.2 | 0.25 x 0.15 | 0.5 | 12 | 0.5 | 0.075 |
| B | Leadless-1 | 7 x 13.6 | 0.35 x 0.7 | 0.8 | 28 | 0.8 | - |
| C | TAB CSP-2 | 7.43 x 5.80 | 0.4 | 0.75 | 40 | 0.885 | 0.3 |
| D | TSOP44 | 18.61 x 10.36 | 0.27 x 0.5 | 0.8 | 44 | 1.13 | n/a |
| E | Leadless-2 | 7 x 12.3 | 0.30 x 0.75 | 0.5 | 46 | 0.8 | n/a |
| F | TAB CSP-1 | 7.87 x 5.76 | 0.4 | 0.75 | 46 | 0.91 | 0.3 |
| G | Chip on Flex-1 (COF-1) | 0.3" x 0.3" | .010 in. | .020 in. | 96 | 1.75 | 0.3 |
| H | CSP-Redistribution-1 | 10.025 x 8.995 | 0.254 | 0.5 | 96 | - | 0.3 |
| I | CSP Redistribution-2 | 6.22 x 5.46 | 0.254 | 0.5 | 99 | - | 0.3 |
| J | Wire Bond on Flex-1 | 12.1 x 12.1 | 0.375 | 0.8 | 144 | 1.4 | 0.5 |
| K | Wire Bond on Flex-2 | 12 x 12 | 0.25 | 0.5 | 176 | 0.5 | 0.3 |
| L | TAB CSP-3 | 13.1 x 13.1 | 0.3 | 0.5 | 188 | 0.5 | 0.3 |
| M | Chip on Flex-2 (COF-2) | 0.5 x 0.5 | .010 in. | .020 in. | 206 | 1.75 | 0.3 |
| N | Ceramic CSP | 15 x 15 | 0.4 | 0.8 | 265 | 0.8 | 0.5 |

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| O | Wafer Level | 0.413 x 0.413 | .010 in. | .020 in. | 275 | - | 0.3 |

* All measurements are in mm unless otherwise specified

**Daisy Chain** — Packages had different pitches, solder ball volumes and compositions, and daisy chain patterns. In most cases, these patterns were irregular and much time and effort was required for design. This was especially cumbersome for packages with higher I/Os and many daisy chain mazes were developed.

**Surface finish** — At least four types of surface finishes were considered. Organic solder preservative (OSP), hot air solder leveling (HASL), Au/Ni (two thicknesses), and immersion silver; the majority were OSP finish. Three types of solder pastes were included: no-clean, water soluble (WS), and rosin mildly activated (RMA).

**Underfill** — Packages with underfill requirements were included both with and without underfill to better understand the reliability consequence of not using underfill.

**Double Sided Assembly** — PWBs were double sided and several boards with double sided packages were assembled to investigate the reliability of single sided versus double sided test vehicles, as well as standard versus microvia technology.

**Solder Volume** — Three stencil thicknesses were included: high, standard, and low. The two extreme thicknesses were 4 and 7 mils with different stencil aperture design depending on the pad size. The standard which was used for the majority of test vehicles was 6 mil thickness.

**Test Vehicle Feature** — The test vehicle was 4.5 by 4.5 inches and divided into four independent regions. For single side assembly, most packages can be cut for failure analysis without affecting the daisy chains of other packages. All packages were daisy chained and they had up to two internal chain patterns.

**Environmental testing** — To link the data to those generated for the Ball Grid Array Consortium test, two conditions of –30° to 100°C (cycle A) and –55° to 125°C (Cycle B) were included. Two additional cycles were also investigated. Thermal cycling in the range of 0° to 100°C was performed to meet the needs of the commercial team members.

Hence, four different thermal cycle profiles were used. These were:

- Cycle A: The cycle A condition ranged from –30° to 100°C and had an increase/decrease heating rate of 2° to 5°C/min and dwell of about 20 minutes at the high temperature to assure near complete creep of the solder. The duration of each cycle was 82 minutes.
- Cycle B: The cycle B condition ranged from –55° to 125°C, with a very high heating/cooling rate. This cycle represent near thermal shock since it utilized a three region chamber: hot, ambient, and cold. Heating and cooling rates were nonlinear with dwells at the extreme temperatures of about 20 minutes. The total cycle lasted approximately 68 minutes.
- Cycle C: The cycle C condition ranged from –55° to 100°C with a short time duration at low temperature. The heating and cooling rates were 2° to 5°C/min with a dwell at maximum temperature of more than 10 minutes.. The duration of each cycle was 90 minutes.
- Cycle D: The cycle D condition ranged from 0° to 100 °C with a 2-5°C/min heating/cooling rate. The Dwell at the extreme temperatures was at least 10 minutes, the cycle duration was 73 minutes.

**Monitoring** — The test vehicles were monitored continuously during the thermal cycles for electrical interruptions and opens. The criteria for an open solder joint specified in IPC-SM-785, Sect. 6.0, were used as guidelines to interpret electrical interruptions. Generally, once the first interruption was observed, there were many additional interruptions within 10% of the cycle life.

## FULL PRODUCTION ASSEMBLY & RELAIBILITY

The Consortium assembled different test vehicle types. For full production, about 150 test vehicles with the many variables discussed above were built. The photograph of an assembled test vehicle, with its packages, face up, is shown in Figure 2. A drawing for the Figure 2 double sided test vehicle in which the back side package outlines are also apparent is shown in Figure 3. Note that a few packages were mirror-imaged to another package in a double sided test vehicle.

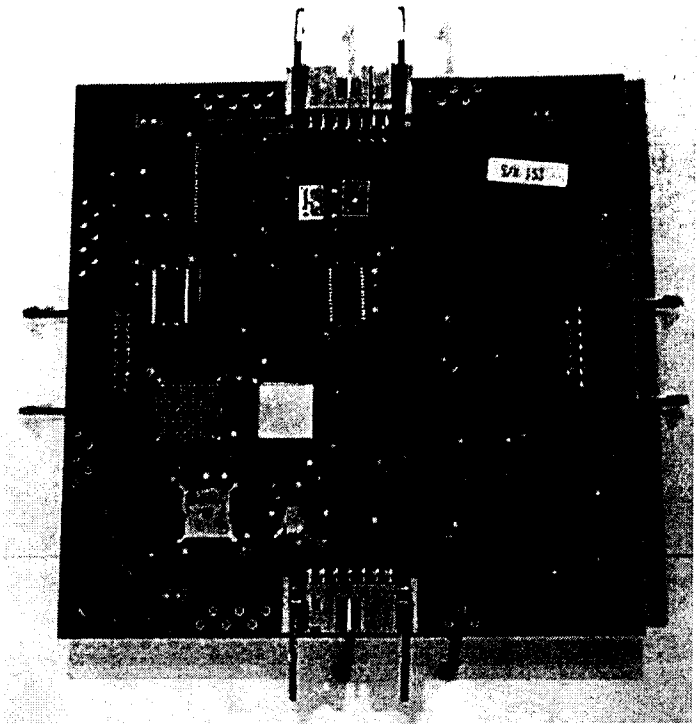

Figure 2 JPL Consortium Test Vehicle, Double Sided

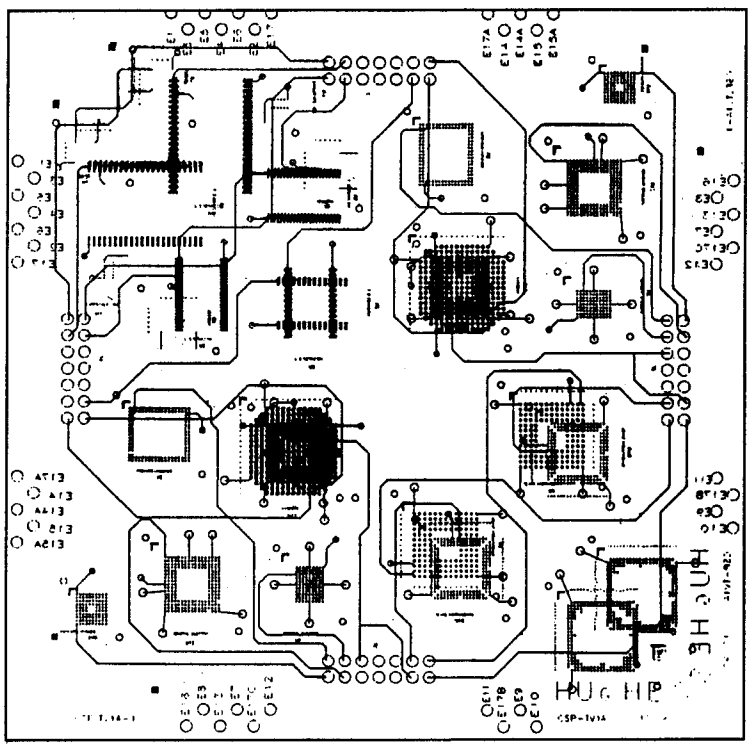

Figure 3 Double Sided Test Vehicle and Regions of Package Overlaps

**Environmental Test Results**

A large number of assemblies have already failed, and their cycles to failure have been documented. Out of these, cycles to failure data for three packages under four thermal cycling conditions are reviewed. Results for two chip on flex assemblies and leadless assemblies on single and double sided test vehicles are also presented.

*Cycles to Failures for Chip on Flex Assemblies*

Figure 4compares cycles to failure test results for the G package with 99 I/Os under four thermal cycling conditions. The trends are as expected, i.e., as the thermal cycling temperature ranges increase, the cycles to failure decrease. Note that assemblies failed between 3 to 34 cycles under a near thermal shock in the range of -55 to 125 °C (B condition). Cycles to failure was 152 cycles under a typical commercial thermal cycling conditions in the ranges of 0 to 100°C. Results for -55/100°C and -30/100°C were between the two extreme cycling conditions as expected.

These data will be used to see the effects of both maximum and minimum temperature changes as well as how well they will follow projection models such as Coffin-Manson relationship.

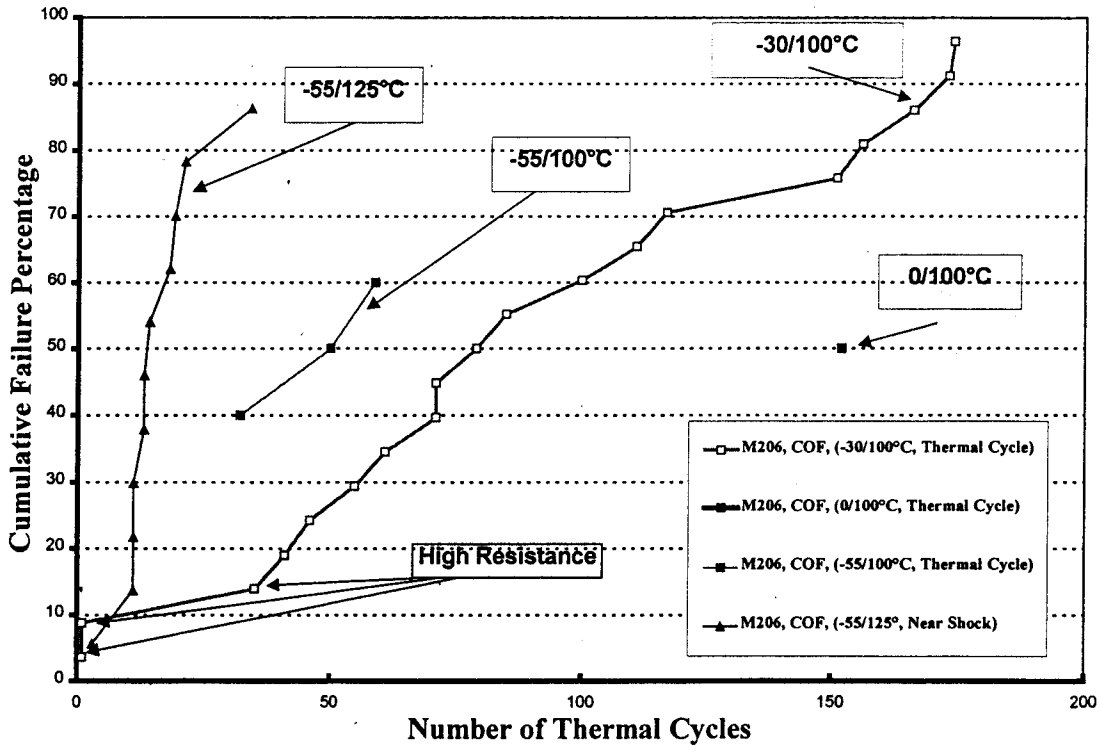


**Figure 4 Cumulative Failure Distribution for Flex on Chip Assemblies with 206 I/Os Under Four Thermal Cycle Conditions**

*X-ray Inspection under Exaggerated Condition*

One M206 assembly which failed at 35 cycles in the range of -30/100 was inspected after it was further cycled to 500. By further cycling, we were able to exaggerate the cracking and separation of solder balls/joint. This allowed the clear observation of solder joint openings that are generally impossible to detect when they have just failed. Figure 5 shows an X-ray photomicrograph of an exaggerated failure. It is apparent that separation occurred either from the package site or board site

*Single and Double Sided Mirror-imaged*

Figure 6 shows thermal cycling test results for package B, a leadless assembly with 28 I/Os, under two conditions for both single and double sided assemblies. The assembly location on the board was such that in a double sided assembly, it was a direct mirror image of itself with a 90° rotation (see Figure 3).

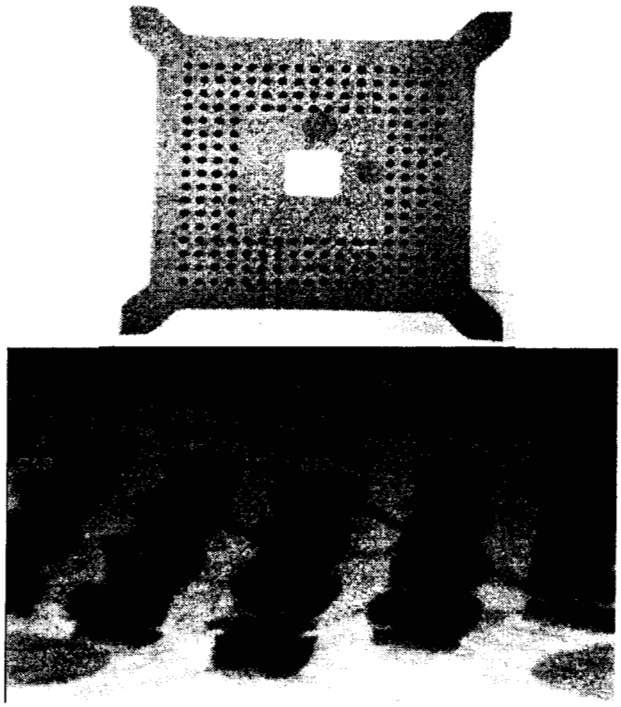

**Figure 5 Exaggerated X-rays showing failure from either package or board sites**

The single sided assemblies failed at much higher cycles that double sided assemblies. The N50 (cycles to 50% failure) were 437 for double and 763 for single sided assemblies under cycle A condition (-30/100 °C). The double sided assemblies also failed much earlier than single sided assemblies under other thermal cycling conditions. As an example, results for double sided assemblies under -55/125°C is also included in the Figure.

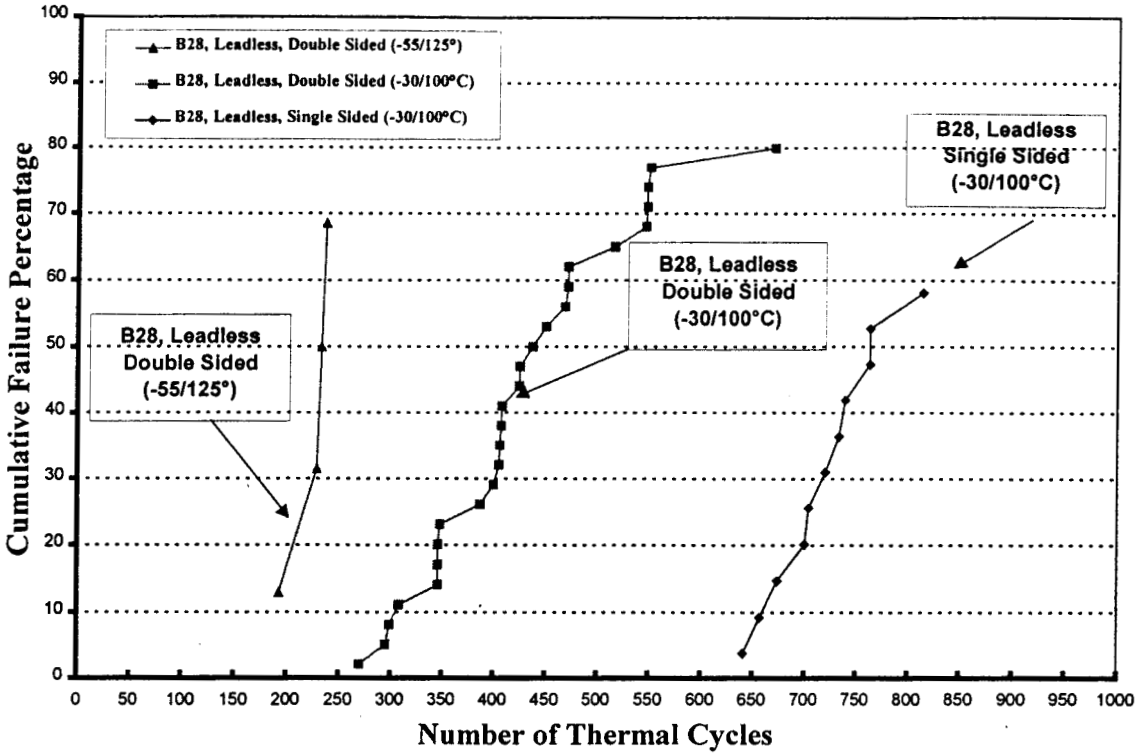


**Figure 6 Single and Double Sided Assembly Failure Comparison**

## DISCUSSION

### Reliability of Single- vs Double-Sided Assemblies

There are many concerns when double sided boards are assembled. Reliability reduction is one. For CSPs, another concern is potential part fall from the assembled side during the second reflow. The small solder volumes; might not generate enough tension force to hold even a small size CSP during second reflow. In addition, it has been shown that for two sided-assemblies with mirror image packages, solder joint reliability was half of the single-sided (Sony, IMAPS '97, Ref 3). Recently, similar test results were presented for another CSP package (Sharp, ECTC '98, Ref. 4). Double sided assemblies with packages on directly opposite sides of the board showed lower cycles to failure. Solder joint reliability increased as the two packages were offset value from mirror position increased.

A similar trend was observed for ceramic CSPs (S. Uegaki, private communications). Several variation including the following were studied.

- Direct overlap and mirror imaged
- Part of package overlap
- No overlap

Both double side assemblies with either direct or corner overlaps showed lower reliability. Reduction in reliability were in the same range as those presented by other authors.

In an effort to determine the cause of the early failure double-sided B28 Leadless assemblies, it was also noticed that this is one of the packages that exactly overlapped another leadless package in the second side with a 90° rotation (see Fig. 8). The lay out for the double sided assembly was not mirror imaged. One image was rotated 90° relative to the first image. During visual examination, it was noticed that the first failure location was at two cross-over corners as shown in Figure ??.. These test results showing early joint failure for double sided assemblies are qualitatively in agreement with those presented earlier.

However, once sets of data recently presented at IPC CSP BGA National Symposium (K. Nakajima, et al., Ref. 5) contradicts the above reliability trend for single and double-sided assemblies. An improvement of 20% for the double-sided assemblies.

For their case, the CSP was mirror imaged with a QFP package on the second side. Increase in board stiffness due to QFP might be one reason for such increase in reliability. I examined the photos given for the both side of their test vehicle design and found that solder joints of the CSP packages were not disturbed by the existence of QFP in the opposite second side. The QFP package was slightly larger than CSP and the leads joints were also on the on the outside periphery of the CSP. It is postulated that when solder joints are directly disturbed, they are affected by double sided assembly. Otherwise, a slight improvement might be achieved due to increase in stiffness.

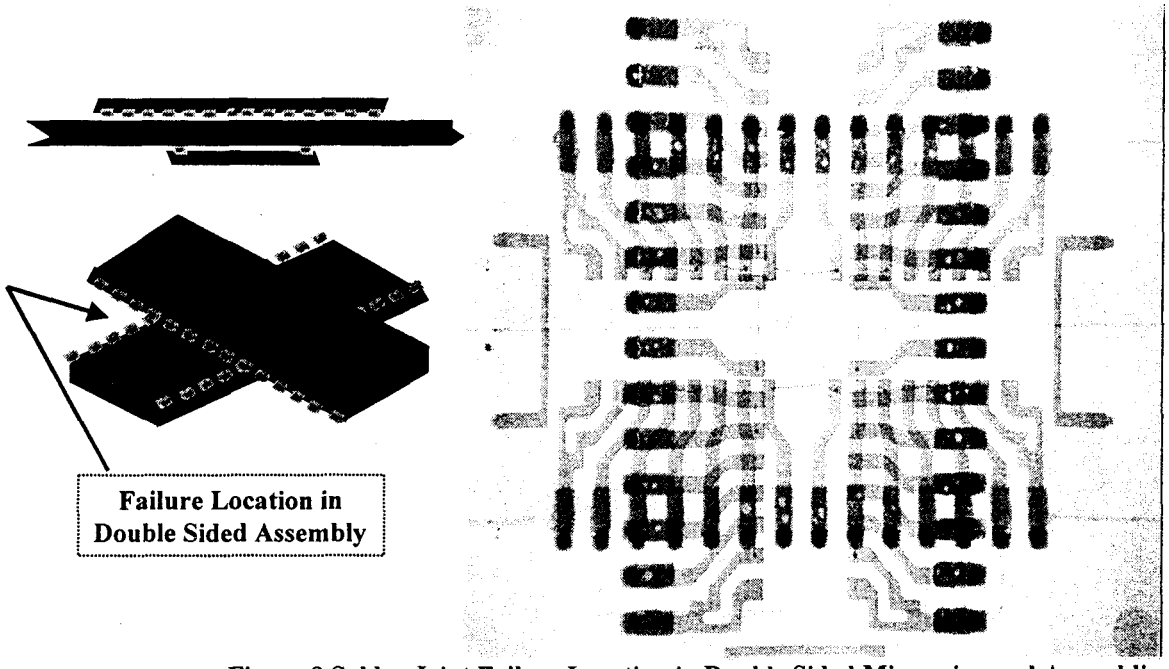


**Figure 8 Solder Joint Failure Location in Double Sided Mirror-imaged Assemblies**

## CONCLUSIONS

- The solder joints which were reflowed twice, in a double sided assembly, showed earlier failures. For a leadless package, this was further worsened by package back to back (mirror image) assembly.
- Cycles to failure for the same assembly under four different environments were different, but the trends were as expected. This means, as temperature cycling ranges increased, cycles to failure decreased.
- One package required underfilling, and three others showed very low cycles to failures. Underfilling might be a requirement for these four packages even for relatively benign commercial application.

For wider CSP implementation, meaningful reliability data are needed. Accelerated thermal cycling might be severe and introduce failure mechanisms that are not representative of field applications. Complimentary tests and failure analyses need to be performed to build confidence in assembly reliability. Thus, understanding the overall philosophy of qualification testing to meet system requirements as well as detecting new failure mechanisms associated with the miniaturized CSPs is the key to collecting meaningful test results and building confidence in its implementation.

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# EDITORIAL ARTICLE

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## CSP RELIABILITY- IS PROVEN?

You might have seen many summary and quotes from the recent publication of NEMI Roadmaps, I thought to add another to your collection. You might have asked the question how this little tiny chip scale package (CSP) are being used especially in portable product could survive all changes in heat and mishandling. You are not alone, expert from NEMI raised a similar question: "BGA and CSPs are attractive from an ease-of-assembly perspective, although reliability to be improved for BGAs and proven for CSPs". This issue on reliability should clarify many questions that you have on CSP and assembly reliability.

Reliability, irrespective of its definition, is no longer an "after-the-fact" concept; rather, it must be an integral part of development and implementation. This is specifically true for microelectronics with demands for miniaturization and system integration in a faster, better, and cheaper environment. CSPs rapid development and introduction into the market is a good example of this trend.

CSPs have their own unique form factor not seen in SMT and many of them may not be able to meet the "traditional" reliability test requirements. There is "paradigm shift" on reliability for CSP and new specific tests such as bend and drop tests are being adopted to especially meet consumer portable requirements. The "shift" is further motivated by several factors including the following:

- Reduction in life expectancy for consumer electronics
- Rapid changes in electronic technology

For surface mount, solder has both electrical and mechanical functions and has been the weakest link in assembly reliability. This means that damage to solder could readily affect functional integrity of the microelectronics system. Therefore, defects that cause changes either in mechanical or electrical system characteristics and understanding their reasons for failure are critical. The most common damage to solder joints are those induced by thermal cycling. Creep and stress relaxation are main causes of cycling damage. Creep for materials generally occurs at temperatures above half of the absolute melting temperature ($T/T_m > 0.5$). This value is 0.65 at room temperature for eutectic solder(63Sn/37Pb).

Thermal damage to solder joints are most often caused by the followings:

- Global CTE (Coefficient of Thermal Expansion) mismatch between the package and board induces stresses. The package and board can also have temperature gradients through the thickness and at surface areas
- Local CTE mismatch between solder attachment to the component and the PWB

Reducing the CTE mismatch of component and PWB reduces cycling damages. For leaded SM package, the CTE mismatch on solder joint was relieved by compliant lead. Rigidity of BGA balls were one of reliability concern at the start of their implementation. Experimental test results showed that BGA assembly failed either between ball and package or ball and PWB (solder joint). For grid CSPs, the interface between package and solder balls is also a potential failure site. These failure mechanisms indicates that package/solder joint shear strength is one of the key parameters that defines package susceptibility to both thermal and mechanical reliability.

Shear strength for BGAs and CSPs were measured and compared. For BGAs, package ball shear values ranged from about 1,000 to 1,500 grams for plastic and ceramic BGAs. These values were the fifty percentile shear forces determined from a large number of ball shear test. For CSPs, shear forces ranged from 170 to about 400 grams. Values for a wafer packages with low I/O (8 Leads) was very low, about 20 g/lead. Shear force depends on many variables including the pad size, metallurgy, and configuration attachment as well a chemistry of solder.

Shear give an indication of deformation susceptibility and especially become critical for application under mechanical conditions. Low values of shear force clearly indicates potential reliability concern with CSPs. However, a few have shown

to survive the short duration shock and vibration requirements. Dynamic behavior are critical especially for application in portable products where there are potential of human mishandling such as accidental drop. Drop test was performed for the UltraCSP™ (P. Elenius, Pan Pacific, '99). Assemblies were dropped from the height of 1600 mm, achieving a mechanical shock of 8200 G over period of 0.12 msec. No failure observed during mechanical shock. No failure was also observed when the drop height increased to 2000 mm with a mechananical shock of 12,500 G over a period of 0.11 msec. Intel reported mechanical shock test results for μBGA™ (R. Bauer, J. Mlatesta, SMI '98) using Mil Std 883. Fifteen samples were subjected to 1500 g with 0.5msec duration in the X, Y, and Z. No failure was observed after five shock pulses. It also showed no failure due to four cycles of vibration in 20-2000 HZ with a 20 g maximum load.

For thermal cycling environment, several features of CSPs had help its reliability. These include reduction in package size and therefore die size and package thicknesses. Both these will improve reliability partially reducing the inherent reliability concern on CSPs. For high reliability applications, especially package with high I/Os, such improvement might not be sufficient and other innovative technology development required in order to decrease the local and global CTE mismatch.

Innovative approaches had been developed aimed at absorbing CTE mismatch between the die and board within the package or externally through strain absorbing mechanisms, and therefore reducing stresses on the solder interconnects. These innovative approaches could introduce their own unique damage mechanisms since possibly the weakest link now has been transferred from solder to other areas of the attachment system. One innovative approach use compliant TAB lead and elastomeric materials between die and substrate to reduce the package CTE mismatch. Since the TABs absorb the majority of stresses, this become the weakest link and possible failure site. This approach has widely shown to be effective for low I/O CSPs, but yet to be proven for higher I/O CSPs. The other innovative approach which is called "Floating Pad Design" has potential for absorbing the global CTE mismatch and therefore, theoretically, it could handle a large I/O package. Test results by manufacturer is promising, but they are yet to be verified by others. It is not know if such solder ball floating would weaken the mechanical strength.

Of course, one undesirable solution to overcome reliability issue is use of underfill. Underfill application is a common technique which has been widely used for direct attachment of chip on board or when package leads are not robust. If everything else failed to improve reliability, this might be the ultimate undesirable solution. This approach for CSP was used by Sony when it introduced its passport size camera in early 1997. Let's review the articles in this issue and see if we need to go that far.